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CMOS Sensor Image-Acquisition and Image- Processing Control System Architecture

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***Abstract*—This report demonstrates an assessment of a PCAM camera module's OV5640 CMOS sensor image-acquisition electrical circuit network system and hardware implementation for associated FPGA-modulated image-processing techniques using Digilent's Zybo Z7-20 development board's FPGA (Zynq 7000 SoC). By comparison between the control system architectures of 2 proposed Active Pixel CMOS sensor electrical network configurations (both 1 Row 1-Column Select Implementations) using electrical network transfer function derivations, time responses, Root Locus Plots, Bode Plots, and their system characteristics as preliminary analyses, FPGA-modulation of the CMOS sensor through image format adjustment is developed as an example of image properties adjustment enabled by the parallel interfacing between Xilinx Vivado, Xilinx SDK, a serial terminal emulator, the FPGA, and the image-processing hardware pipeline.**

***Index Terms*—CMOS sensor, image-acquisition, image-processing, control system architecture, Laplacian Transform, time response, Root Locus, Bode Plot, Simulink, MatLab, Transfer Function, SCCB, FREX, MIPI, computer architecture, IP Core, FPGA, photodiode, MOSFETs, gain amplifier, camera electronics, electrical circuit network system, Zybo Z7-20, Zynq 7000 SoC, Xilinx Vivado, Vivado SDK, serial terminal emulator, RAW to RGB, image format adjustment, FPGA modulation**

I. Introduction

THIS REPORT is a technical paper for *CMOS Sensor Image-Acquisition and Image-Processing Control System Architecture*, completed for the Final Project required by the course EE405: Control Systems I at University of North Dakota. It includes the circuit schematics, Laplacian derivations of the system's transfer function, control feedback equivalent representations, implementations of the transfer function method in Simulink for the time responses, and MatLab scripts for the Root Locus and Bode Plots for the 2 CMOS sensor configurations. Configuration 1 is unique in that it has a unity feedback $H(s) = 1$ while Configuration 2 has a non-unity feedback that includes electrical network variables. The values of the variables are assumed so as to obtain readable time responses and plots. The systems' stability conditions are analyzed according to K values. Data tables include the circuits' parameters and system characteristics. Lastly, the project implements hardware-software application, analysis of the computer for understanding cascaded systems working in parallel in the closed-loop pipeline, and an example of image properties adjustment through FPGA-modulation after additional exploration of the theory behind a possible state-space model for the CMOS sensor pixel color-space conversion. *Note:* Fundamental control systems concepts are developed from "Control Systems Engineering, Seventh Edition," by Norman S. Nise.

II. Active Pixel CMOS Sensor Image-acquisition Electrical Network (1 row-1 column configuration 1: Unity Feedback)

A. *Circuit Schematic*

The Active Pixel CMOS Sensor Image-Acquisition Electrical Network (before ADC) for Configuration 1 includes 3 P-Channel MOSFETs, a photodiode, and a terminal amplifier. The photodiode is light sensitive as it detects photonic energy and converts it into electrical charge that produces current; the current is processed through the transimpedance amplifier configuration as part of the feedback network. The three MOSFETs are considered as the M_{rst} for the photodiode reset, M_{sf} for light charge to voltage amplification, and M_{sel} for row select. The non-inverting output gain amplifier amplifies voltage before analog-digital conversion; The transimpedance configuration incorporating the photodiode allows for acceptance of current to transform it into an analog voltage before the gain is turned into a digital voltage for image-processing on a computational system. The CMOS Sensor network includes a transimpedance amplifier that, along with the feedback photodiode, can convert photo-current into voltage as a "pixel processer."

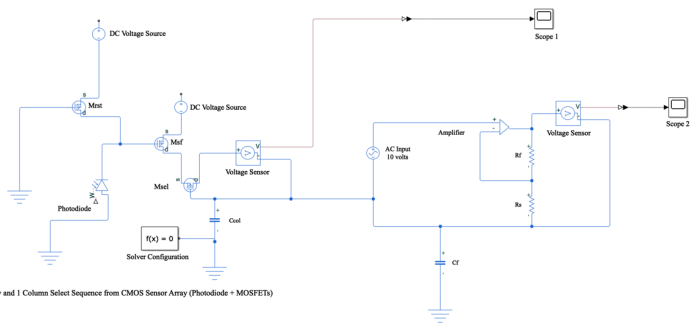


Figure 1. Active Pixel CMOS Sensor Image-Acquisition Electrical Network (1 Row-1 Column Configuration 1)

*B. **Laplacian Derivation of the System's Transfer Function***

For simplification, the following Laplacian Linearization of such a non-linear system considers the real voltage multiples of the transimpedance and switching components' equations as design parameter constants *outside* of the effective time-domain functions required for Laplacian transformation into the *s*-domain. The equation solved for the highest-order derivative is obtained using the voltage-charge relations from *Table 2.3 (Nise)* with: [1] **CMOS Sensor MOSFETs**, [2] **Transimpedance Photodiode** for light input conversion, and [3] **Non-Inverting Transimpedance Amplifier** (assuming zero initial conditions):

[1] **Photodiode:** $H(s)$:
From the output feedback factor of the transimpedance photodiode;
$H(j\omega) = \left[\frac{1 + j\omega(R_F C_F)}{1 + j\omega R_F (C_F)}\right]$
and substituting Laplacian *s* for each $j\omega$:
$H(s) = \left[\frac{1 + s(R_F C_F)}{1 + sR_F (C_F)}\right]$
$$\boldsymbol{H(s) = \frac{1 + R_F C_F s}{1 + R_F C_F s} = 1} \text{ (unity feedback)} \quad (1)$$

[2] **MOSFETs:** $G_1(s)$:
From $\left[\frac{I_P}{|V_{OV}|}\right]\left[\frac{I}{|V_{OV}|}\right](V_{rst} - V_{sig})$;
Upon application of admittance Laplacian relationships for the substitutable electrical components,
$$\boldsymbol{G_1(s) = (Cs)(Cs) = C^2 s^2} \quad (2)$$

[3] **Non-Inverting Output Gain Amplifier:** $G_2(s)$:
From $(V_{amp})\left[\frac{R_S + R_F}{R_S}\right] = (V_{amp})\left[1 + \frac{R_F}{R_S}\right]$;
Upon application of admittance Laplacian relationships for the substitutable electrical components,
$$\boldsymbol{G_2(s) = 1 + \frac{R_S}{R_F}} \quad (3)$$

Since the MOSFETs network and the Non-Inverting Output Gain Amplifier network are considered cascaded:

$$\boldsymbol{G(s)} = G_1(s)G_2(s) = [C^2 s^2]\left[1 + \frac{R_S}{R_F}\right]$$
$$= \left[C^2 S^2 + \frac{C^2 s^2 R_S}{R_F}\right]$$
$$= \boldsymbol{\frac{C^2 R_F s^2 + C^2 s^2 R_S}{R_F}} \quad (4)$$

With
$H(s) = 1$ and (1)
$G(s) = G_1(s)G_2(s) = \frac{C^2 R_F s^2 + C^2 s^2 R_S}{R_F}$, (4)
The CMOS Sensor system transfer function is:

$$\boldsymbol{T(s)} = \frac{\frac{o}{p}}{\frac{i}{p}} = \frac{G(s)}{1 + G(s)H(s)}$$
$$= \frac{\left[\frac{C^2 R_F s^2 + C^2 s^2 R_S}{R_F}\right]}{1 + \left[\frac{C^2 R_F s^2 + C^2 s^2 R_S}{R_F}\right][1]}$$
$$= \frac{[C^2 R_F + C^2 R_S]s^2}{[C^2 R_F + C^2 R_S]s^2 + R_F} \quad (5)$$

Assuming values for the variables of the system:
$R_F = 10\ k\Omega$
$R_s = 1\ k\Omega$
$C = 25\ F$ (as C_{col} from column select)
$C_F = 75\ F$

With assumed values of component variables:
$$T(s) = \frac{[(25)^2(10k) + (25)^2(1k)]s^2}{[(25)^2(10k) + (25)^2(1k)]s^2 + (10k)} \quad (6)$$

Implemented in Simulink in the most reduced form is the CMOS Sensor system transfer function below:
$$\boldsymbol{T(s) = \frac{[6875000]s^2}{[6875000]s^2 + 10E3}} \quad (7)$$

*C. **Control Feedback System Representation, Transfer Function Method in Simulink, and Time Responses***

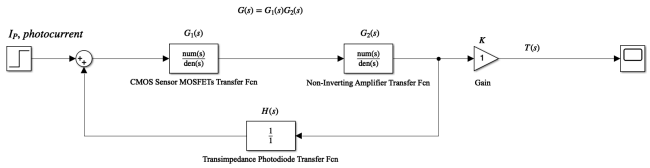


Figure 2. Control Feedback System Representation (Configuration 1)

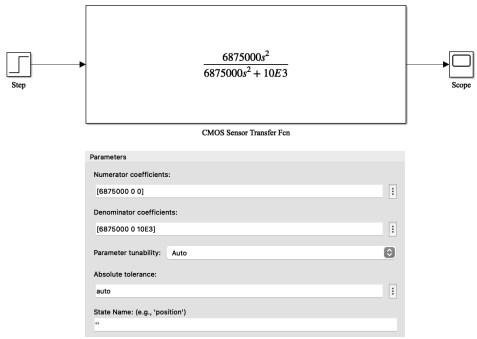


Figure 3. Transfer Function Method in Simulink to obtain Time Response (Configuration 1)

In Simulink, the Configuration 1 system is simulated over a 50 second period using the derived transfer function.

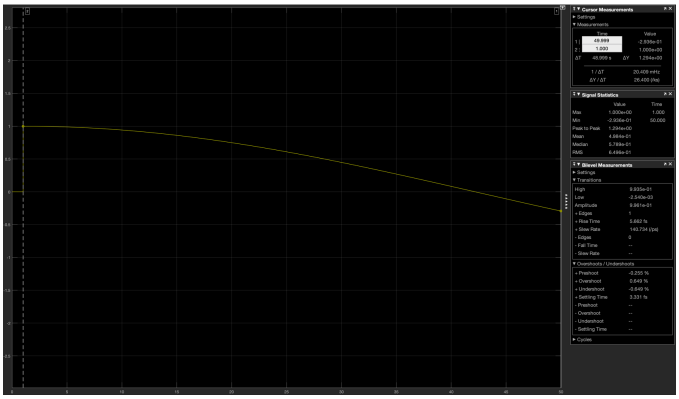


Figure 4. Standard Time Response from Configuration 1

For Steady-State Error time responses, Step-Input, Ramp-Input, and Parabolic Input were simulated 50 second time periods:

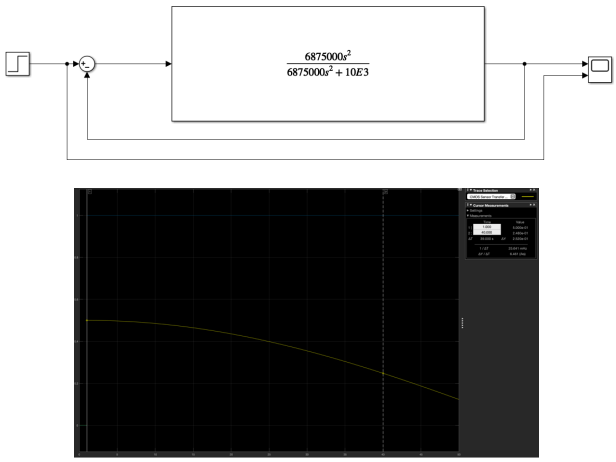


Figure 5. Step Input Steady-State Error (Configuration 1)

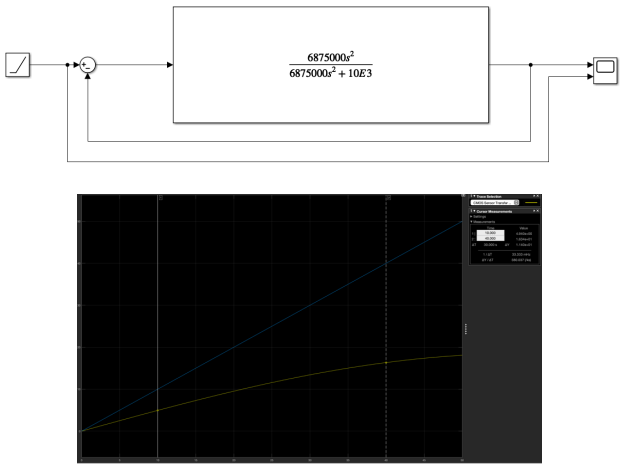


Figure 6. Ramp Input Steady-State Error (Configuration 1)

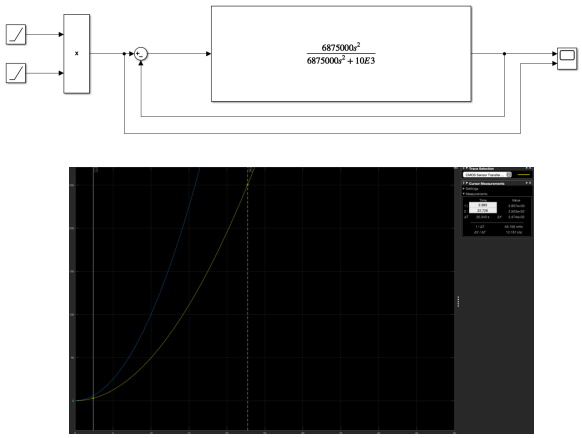


Figure 7. Parabolic Input Steady-State Error (Configuration 1)

D. *MatLab scripts, Root Locus Plots, and Bode Plots*

The MatLab script for a continuous time-transfer function is implemented into Control System Designer to obtain the reference Root Locus Plot:

```
>> s = tf('s')

s =

  s

Continuous-time transfer function.

>> sys = ((6875000)*(s^2))/((6875000)*(s^2) + 10000)

sys =

      6.875e06 s^2
  --------------------
  6.875e06 s^2 + 10000

Continuous-time transfer function.

>> controlSystemDesigner(sys)
```

Figure 8. MatLab script for transfer function of CMOS Sensor Electrical Network Configuration 1

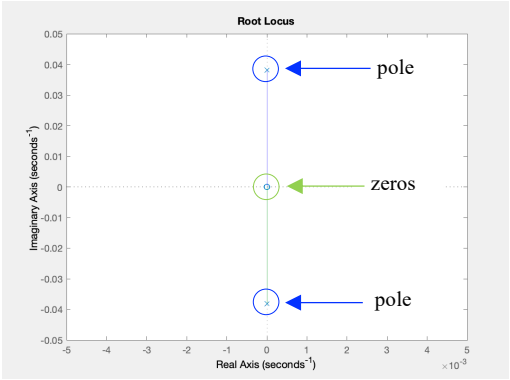


Figure 9a. Root Locus Plot (CMOS Sensor Electrical Network Configuration 1) for $K = 1$

Upon initial generation of the Root Locus Plot, it seems all roots are on the imaginary axis. However, through maximization of the graphical scale and use of the interpolation function, it is found that the Root Locus Plot has 2 poles on the imaginary axis and 2 zeros on the real axis:

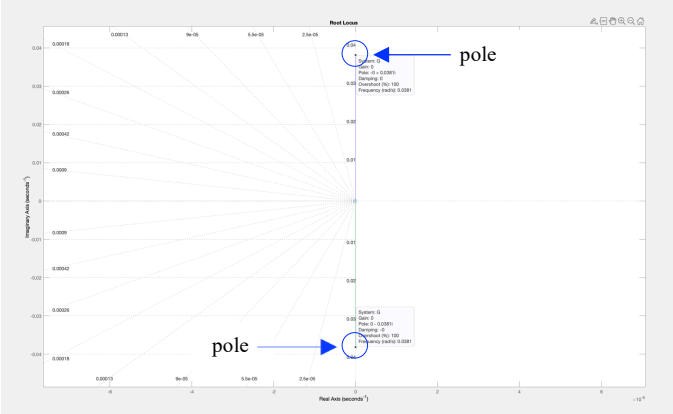


Figure 9b. Root Locus Plot (CMOS Sensor Electrical Network Configuration 1) for $K = 1$ showing the 2 poles on the imaginary axis

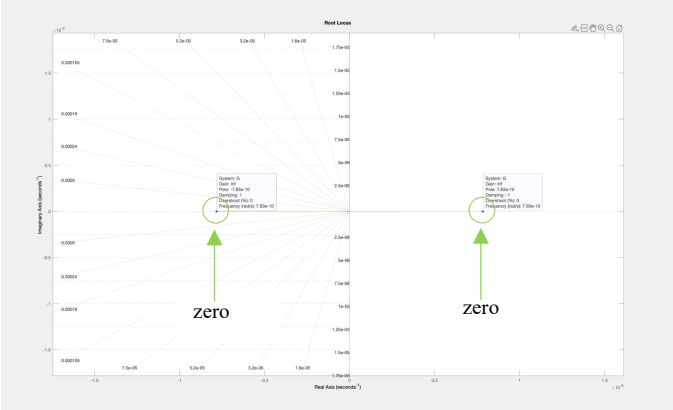


Figure 9c. Root Locus Plot (CMOS Sensor Electrical Network Configuration 1) for $K = 1$ showing the 2 zeros on the real axis

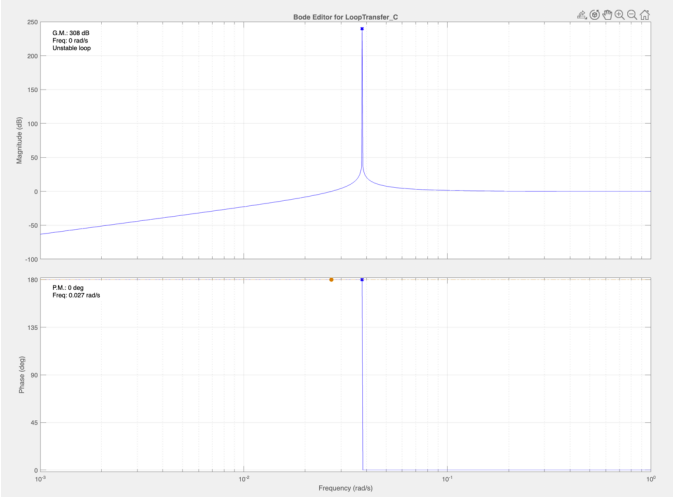


Figure 10. Bode Plot (CMOS Sensor Electrical Network Configuration 1) for $K = 1$

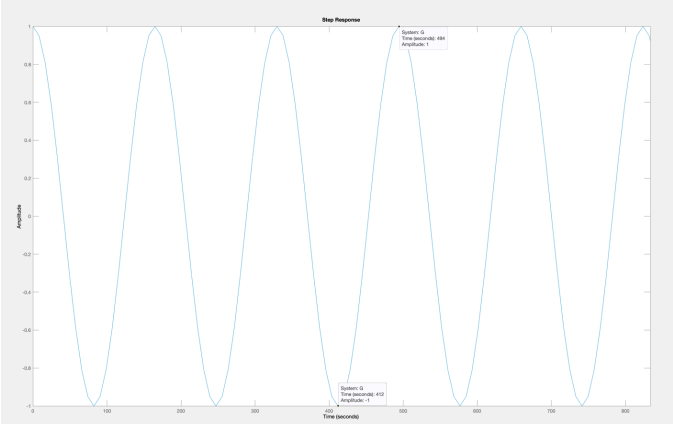


Figure 11. Step Response (CMOS Sensor Electrical Network Configuration 1) for $K = 1$

This system is marginally stable. Using the poles equation, the system can be classified as undamped by solving for $\zeta = 0$ through Equation (4.24):

$$s_{1,2} = -\zeta\,\omega_n \pm \omega_n\sqrt{\zeta^2 - 1} \qquad \text{(4.24, Nise)}$$

For this unique case, the Routh-Hurwitz Criterion can be implemented to find the conditional value of K which determines the system stability by using the characteristic equation $[6875000]s^2 + 10000 + K = 0$:

$\boldsymbol{s^2}$	6875000	10000
$\boldsymbol{s^1}$	$\theta \to \Sigma \ll 0.001$	K
$\boldsymbol{s^0}$	$\left[\frac{(\Sigma)(10000) - (6875000)K}{\Sigma}\right]$	

$\left[\frac{(\Sigma)(10000) - (6875000)K}{\Sigma}\right] > 0$ for system stability.

$$(\Sigma)(10000) - (6875000)K > 0$$
$$(0.001)(10000) - (6875000)K > 0$$
$$10 - (6875000)K > 0$$
$$-(6875000)K > -10$$
$$\boldsymbol{K > \frac{10}{6875000}} \text{ for system stability.} \qquad (8)$$

To understand how the system characteristics would be affected when the K value is changed to meet the condition of $K < \frac{10}{6875000}$ for testing a K value that makes the system unstable, the plots and time response were analyzed for $K = -10$. Using equation 4.24, the system can still be classified as undamped by solving for $\zeta = 0$. The Step Response generated for $K = -10$ demonstrates the most apparent difference from when gain was greater than the point between instability and stability in that the curved slope tended toward the peak amplitude in what seems to be an exponential way rather than oscillate over time as the system did for the $K = 1$ Step Response.

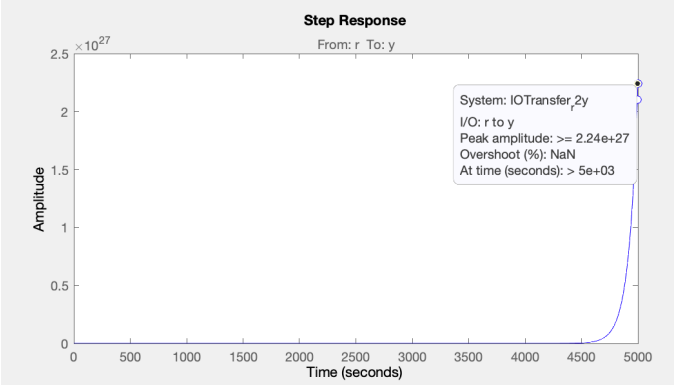


Figure 12. Step Response (CMOS Sensor Electrical Network Configuration 1) for $K = -10$

For sake of brevity and since the rest of the plots look fairly similar to those for $K = -10$, the remaining results are collected and summarized in Table 2.

III. Active Pixel CMOS Sensor Image-Acquisition Electrical Network (1 row-1 column configuration 2: Non-Unity Feedback)

A. *Circuit Schematic*

Configuration 2 of the CMOS Sensor Image-Acquisition Electrical Network circuit is still 1 Row-1 Column; However, in comparison to Configuration 1, Configuration 2 has additional electrical components to result in a non-unity feedback, as explained through the derivation of the transfer function.

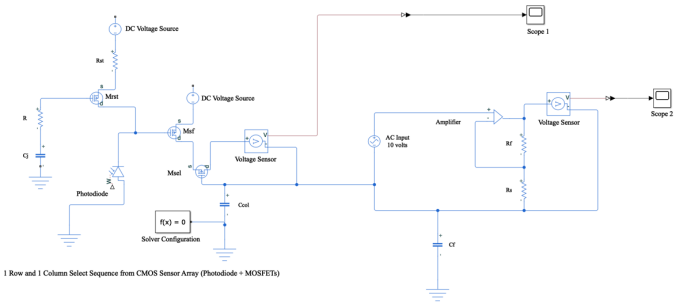


Figure 13. Active Pixel CMOS Sensor Image-Acquisition Electrical Network (1 Row-1 Column Configuration 2)

B. *Laplacian Derivation of the System's Transfer Function*

[1] Photodiode: $H(s)$:

From the output feedback factor of the transimpedance photodiode;

$$H(j\omega) = \left[\frac{1 + j\omega(R_F C_F)}{1 + j\omega R_F(C_j + C_F)}\right] \tag{9}$$

and substituting Laplacian s for each $j\omega$:

$$H(s) = \left[\frac{1+s(R_F C_F)}{1+sR_F(C_j + C_F)}\right] = \frac{\mathbf{1 + R_F C_F s}}{\mathbf{1 + R_F C_j s + R_F C_F s}} \tag{10}$$

[2] MOSFETs: $G_1(s)$:

From $\left[\frac{I_P R}{|V_{OV}|}\right]\left[\frac{I R_{st}}{|V_{OV}|}\right](V_{rst} - V_{sig})$; (11)

Upon application of admittance Laplacian relationships for the substitutable electrical components,

$$G_1(s) = Cs\left(\frac{1}{R}\right) Cs\left(\frac{1}{R_{st}}\right) = \mathbf{C^2 s^2}\left(\frac{\mathbf{1}}{\mathbf{RR_{st}}}\right) \tag{12}$$

[3] Non-Inverting Output Gain Amplifier: $G_2(s)$:

From $(V_{amp})\left[\frac{R_S + R_F}{R_S}\right] = (V_{amp})\left[1 + \frac{R_F}{R_S}\right]$; (13)

Upon application of admittance Laplacian relationships for the substitutable electrical components,

$$G_2(s) = \mathbf{1} + \frac{\boldsymbol{R_S}}{\boldsymbol{R_F}} \tag{14}$$

Since the MOSFETs network and the Non-Inverting Output Gain Amplifier network are considered cascaded:

$$\begin{aligned} \boldsymbol{G(s)} = G_1(s)G_2(s) &= \left[\frac{C^2 s^2}{RR_{st}}\right]\left[1 + \frac{R_S}{R_F}\right] \\ &= \left[\frac{C^2 s^2}{RR_{st}} + \frac{C^2 s^2 R_S}{RR_{st}R_F}\right] \\ &= \frac{\boldsymbol{C^2 R_F s^2 + C^2 s^2 R_S}}{\boldsymbol{RR_{st}R_F}} \end{aligned} \tag{15}$$

$$H(s) = \frac{1 + R_F C_F s}{1 + R_F C_j s + R_F C_F s} \text{ and} \tag{10}$$

$$G(s) = G_1(s)G_2(s) = \frac{C^2 R_F s^2 + C^2 s^2 R_S}{RR_{st}R_F}, \tag{15}$$

The CMOS Sensor system transfer function is:

$$\begin{aligned} \boldsymbol{T(s)} = \frac{\frac{o}{p}}{\frac{i}{p}} &= \frac{G(s)}{1 + G(s)H(s)} \\ &= \frac{\left[\frac{C^2 R_F s^2 + C^2 s^2 R_S}{RR_{st}R_F}\right]}{1 + \left[\frac{C^2 R_F s^2 + C^2 s^2 R_S}{RR_{st}R_F}\right]\left[\frac{1 + R_F C_F s}{1 + R_F C_j s + R_F C_F s}\right]} \\ &= \frac{[C^2 R_F^2 C_j + C^2 R_F R_s C_j + C^2 R_F^2 C_F + C^2 R_F C_F R_s]s^3 + [C^2 R_F + C^2 R_s]s^2}{[C^2 R_F^2 C_F + C^2 C_F R_F R_s]s^3 + [C^2 R_F + C^2 R_s]s^2 + [RR_{st}R_F^2 C_j + RR_{st}R_F^2 C_F]s + [RR_{st}R_F]} \end{aligned} \tag{16}$$

Assuming values for the variables of the system:

$R = 500\ \Omega$
$R_{st} = 150\ \Omega$
$R_F = 10\ k\Omega$
$R_s = 1\ k\Omega$
$C = 25\ F$ (as C_{col} from column select)
$C_F = 75\ F$
$C_j = 100\ F$

With assumed values of component variables:

$$T(s) = \frac{[(25)^2(10k)^2(100) + (25)^2(10k)(1k)(100) + (25)^2(10k)^2(75) + (25)^2(10k)(75)(1k)]s^3 + [(25)^2(10k) + (25)^2(1k)]s^2}{[(25)^2(10k)^2(75) + (25)^2(75)(10k)(1k)]s^3 + [(25)^2(10k) + (25)^2(1k)]s^2 + [(500)(150)(10k)^2(100) + 500)(150)(10k)^2(75)]s + [(500)(150)(10k)]} \tag{17}$$

Implemented in Simulink in the most reduced form is the CMOS Sensor system transfer function below:

$$\boldsymbol{T(s)} = \frac{\mathbf{[1.203125E13]s^3 + [6875000]s^2}}{\mathbf{[5.15625E12]s^3 + [6875000]s^2 + [1.3125E15]s + [750000000]}} \tag{18}$$

C. *Control Feedback Equivalent Representation, Transfer Function Method in Simulink, and Time Reponses*

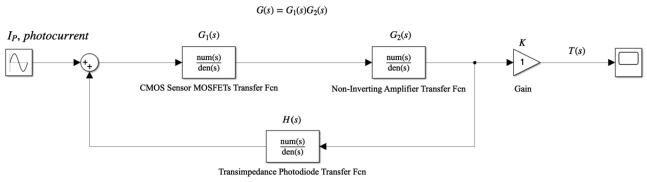


Figure 14. Control Feedback System Representation (Configuration 2)

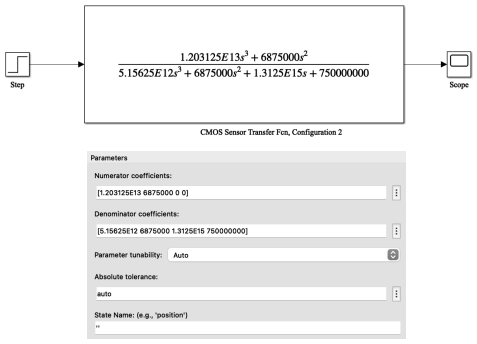
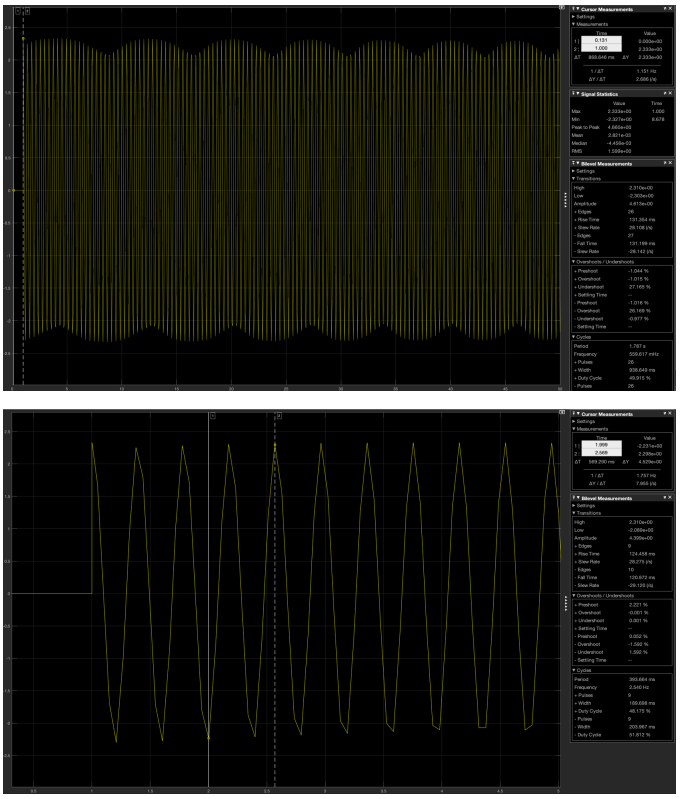


Figure 15. Transfer Function Method in Simulink to obtain Time Response (Configuration 2)

In Simulink, the Configuration 2 system is simulated over a 50 second period using the derived transfer function.



Figures 16a-b. Standard Time Response from Configuration 2 (with 16b showing maximum and minimum values for steady-state oscillations)

For Steady-State Error time responses, Step-Input, Ramp-Input, and Parabolic Input were simulated over 20 second time periods:

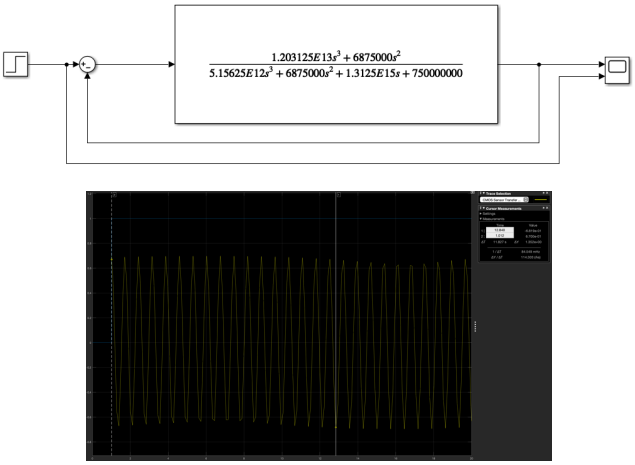


Figure 17. Step Input Steady-State Error (Configuration 2)

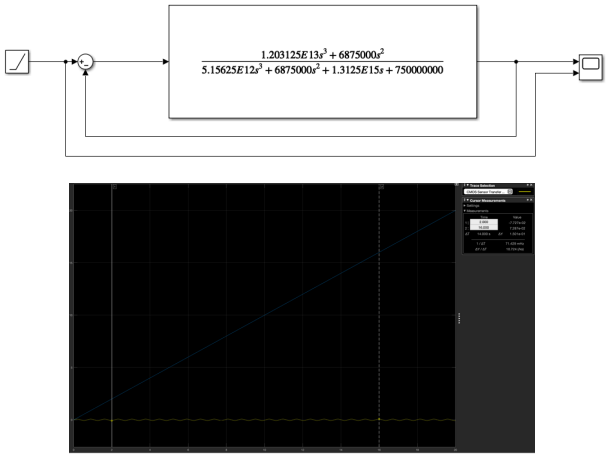


Figure 18. Ramp Input Steady-State Error (Configuration 2)

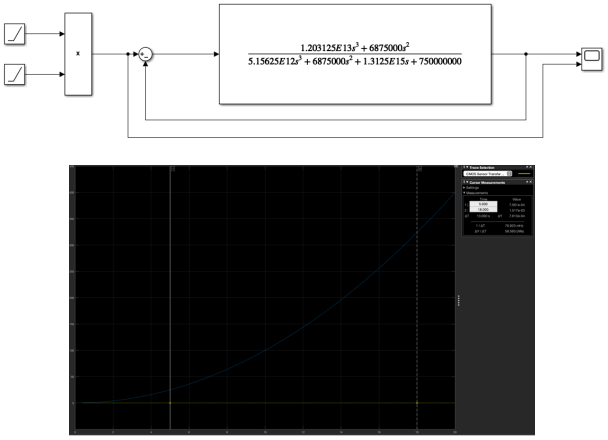


Figure 19. Parabolic Input Steady-State Error (Configuration 2)

D. MatLab scripts, Root Locus Plots, and Bode Plots

The MatLab script for a continuous time-transfer function is implemented into Control System Designer to obtain the reference Root Locus Plot:

```
>> s = tf('s')

s =

  s

Continuous-time transfer function.

>> sys = ((1.203125e13)*(s^3) + (6875000)*(s^2))/((5.15625e12)*(s^3) + (6875000)*(s^2) + (1.3125e15)*(s) + 750000000)

sys =

             1.203e13 s^3 + 6.875e06 s^2
  ------------------------------------------------------
  5.156e12 s^3 + 6.875e06 s^2 + 1.312e15 s + 7.5e08

Continuous-time transfer function.

>> controlSystemDesigner(sys)
```

Figure 20. MatLab script for transfer function of CMOS Sensor Electrical Network Configuration 2

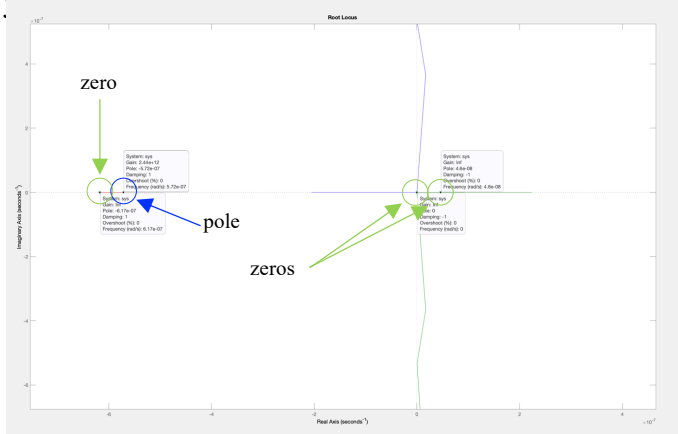


Figure 21a. Root Locus Plot (CMOS Sensor Electrical Network Configuration 2) for $K = 1$ showing real axis roots

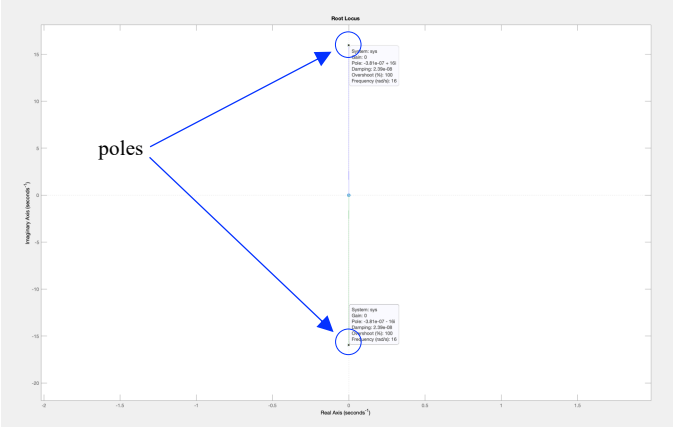


Figure 21b. Root Locus Plot (CMOS Sensor Electrical Network Configuration 2) for $K = 1$ showing imaginary axis roots

For $K = 1$, the system has 3 zeros and 1 pole on the real axis and 2 poles on the imaginary axis.

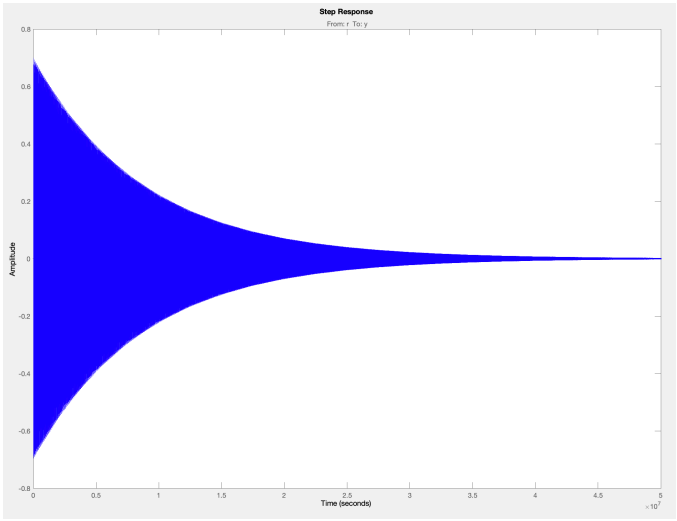


Figure 22a. Step Response Plot (CMOS Sensor Electrical Network Configuration 2) for $K = 1$

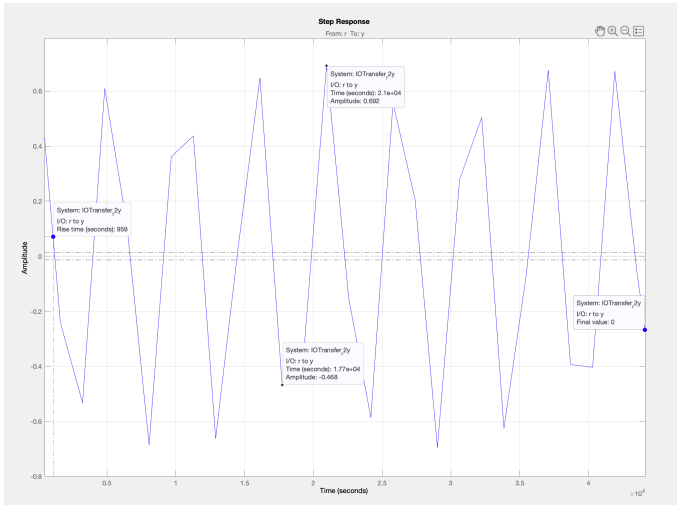


Figure 22b. Close up Step Response (CMOS Sensor Electrical Network Configuration 2) for $K = 1$ showing peak amplitude, minimum amplitude, rise time, and settling time

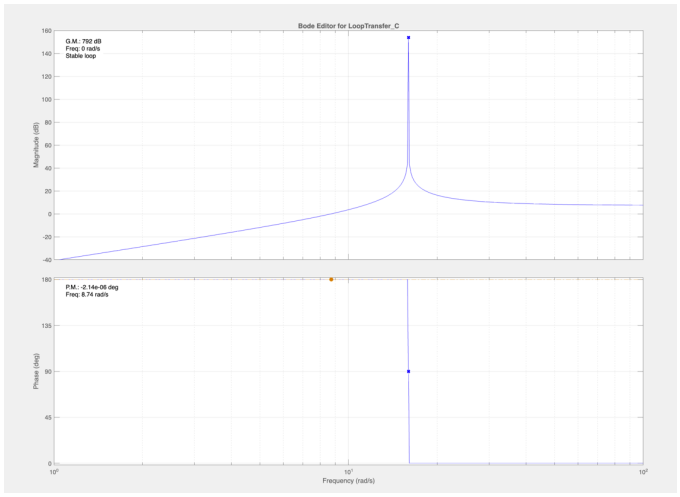


Figure 23. Bode Plot (CMOS Sensor Electrical Network Configuration 2) for $K = 1$

This system is underdamped with $0 < \zeta < 1$ and theoretically, the oscillations are not supposed to reach a point at which it ends its oscillations.

The Routh-Hurwitz Criterion can be implemented to find the conditional value of K which determines the system stability by using the characteristic equation $[5.15625E12]s^3 + [6875000]s^2 + [1.3125E15]s + 750000000 + K = 0$: (19)

$\boldsymbol{s^3}$	$5.15625E12$	$1.3125E15$
$\boldsymbol{s^2}$	6875000	750000000
$\boldsymbol{s^1}$	K	0
$\boldsymbol{s^0}$	750000000	0

This system is stable for all values of $K > 0$. The plots and time response for the system with $K = -10$ is explored to see how the system would be affected when the gain makes it unstable.

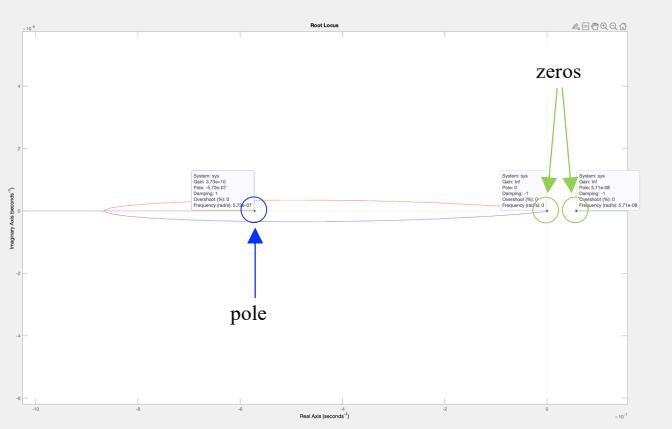


Figure 24. Root Locus Plot (CMOS Sensor Electrical Network Configuration 2) for $K = -10$ showing 1 pole and 2 zeros on the real axis

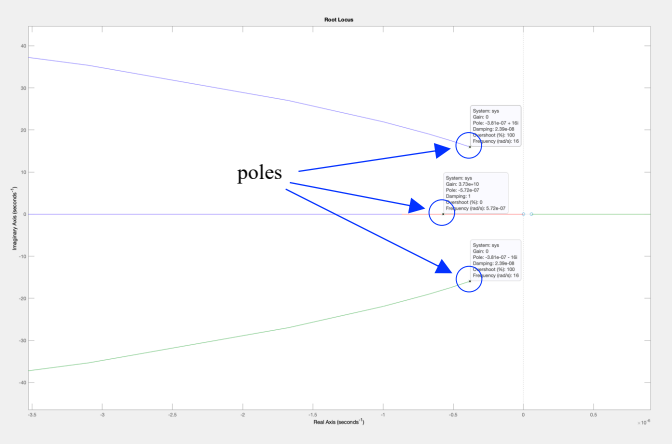


Figure 25. Root Locus Plot (CMOS Sensor Electrical Network Configuration 2) for $K = -10$ showing the total of 3 poles

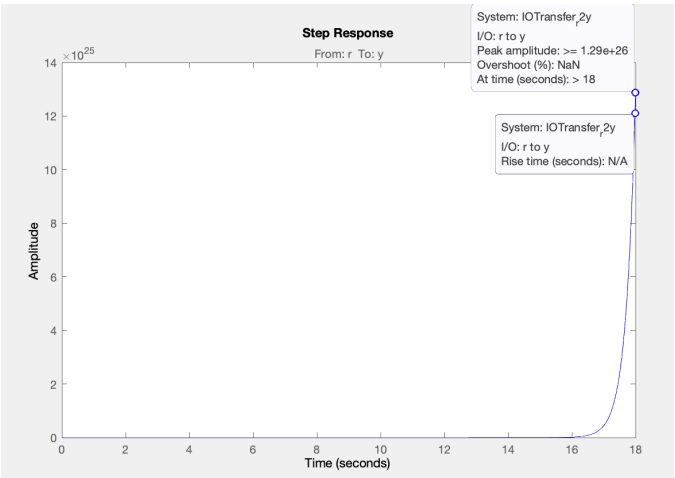


Figure 26. Step Response (CMOS Sensor Electrical Network Configuration 2) for $K = -10$

For $K = -10$, the system has 2 obvious zeros and 1 pole on the real axis and 2 other poles on the *s*-plane. The third zero may be from the overlap at the 0 origin. For sake of brevity, the remaining data for the Configuration 2 system with $K = -10$ is shown on Table 2.

V. Data Tables: Simulated Components and Electrical Network Transfer Function Relationships

Circuit Component	Abbreviation	Value
Resistor	R	500 Ω
Resistor, reset	R_{st}	150 Ω
Resistor, feedback	R_f	10 kΩ
Resistor, select	R_s	1 kΩ
Capacitor, column select	C or C_{col}	25 F
Capacitor, feedback	C_f	75 F
Capacitor, junction	C_j	100 F
MOSFET, Photodiode Reset	M_{rst}	
MOSFET, Light Charge To Voltage Amplification	M_{sf}	
MOSFET, Row Select	M_{sel}	

Figure 27. Simulated Electrical Network Components Table

Circuit Component	Impedance, $Z(s) = \frac{V(s)}{I(s)}$	Admittance, Y(s) = I(s)/V(s)
Photodiode	$\frac{1}{Cs}$	Cs
MOSFET	R, $\frac{1}{Cs}$	$\frac{1}{R}$ = G, Cs
Amplifier	R	$\frac{1}{R}$ = G
Resistor	R	$\frac{1}{R}$ = G
Capacitor	$\frac{1}{Cs}$	Cs

Figure 28. Electrical Network Transfer Function Relationships; used in the Laplacian derivations of transfer functions representing CMOS Sensor electrical networks; abstracting from the voltage-charge relations (Nise) and from equivalent circuit representation equations (Bhat)

VI. Collected Data Tables: System Characteristics

A. Table 1: $K = 1$ *(Reference)*

K = 1			
CMOS Sensor Electrical Network		Configuration 1: Unity Feedback	Configuration 2
Data Type	Parameter		
1. Time Response			
	Rise Time (s)	0.3046	959
	Peak Time (s)	0.204	2.10E+04
	Peak Amplitude	1	0.692
	Overshoot	0.483%	0%
	Undershoot	1.7%	0%
	Final Value, max	1	0
	Final Value, min	-1	0
2. Bode Plot			
	Gain Margin (dB)	308	792
	Phase Margin (deg)	0	-2.14E-06
	Frequency (rad/s)	0.027	8.74
	Stability	Marginally Stable	Stable
3. Root Locus			
	Poles	0 ± j0.0381	-0.000000381 ± j16, -5.72E-07
	Zeros	± 7.83E-10	-6.17E-07, 0, 4.6E-08
	Damping Ratio, ζ	0	0 < ζ <1
	Natural frequency, ωn	± 0.0381	± 16
	System Classification	Undamped	Underdamped

Figure 29. Table 1: System Characteristics for $K = 1$

B. **Table 2: $K = -10$**

K = -10			
CMOS Sensor Electrical Network		**Configuration 1: Unity Feedback**	**Configuration 2**
Data Type	**Parameter**		
1. Time Response			
	Rise Time (s)	N/A	N/A
	Peak Time (s)	5.E+03	> 18
	Peak Amplitude	2.24E+27	>= 1.29E+26
	Overshoot	NaN	NaN
	Undershoot	1.7%	N/A
	Final Value, max	Inf	Inf
	Final Value, min	N/A	N/A
2. Bode Plot			
	Gain Margin (dB)	-20	-27.4
	Phase Margin (deg)	-180	-180
	Frequency (rad/s)	0.0115	3.23
	Stability	Unstable	Unstable
3. Root Locus			
	Poles	0 ± j0.0386	-3.81E-07 ± j16, -5.72E-07
	Zeros	0 ± j0	± 0, 6.29E-08
	Damping Ratio, ζ	0	0 < ζ <1
	Natural frequency, ωn	± 0.0386	± 16
	System Classification	Undamped	Underdamped

Figure 30. Table 2: System Characteristics for $K = -10$

VII. Experimental Application

A. ***CMOS Sensor + Amplifier Image-Acquisition FPGA-Modulated Feedback Control System Block Diagram***

In parallel are the 3 cascaded systems during FPGA modulation of acquired pixels that may be outputted when making computational adjustments to image properties such as resolution or image format or processes such as reading and writing register addresses to the CMOS sensor: [1] *Pixel-Acquisition*: Light input through lens > FREX pin (frame exposure and mechanical shutter, "pre-exposure") > Timing Generator and System Control Logic > Control Bus > Sensor array (Pixel "Sampling") > Amplifier > ADC, [2] *Image-Generation*: ISP > FIFO > Data Output via DVP, and [3] *Image-Properties Modification Read-Out*: Xilinx Vivado Software System > Zynq 7000 SoC FPGA > SCCB Interface at CMOS Sensor Unit > Control Register Bank > Control Bus > FIFO > Data Output via DVP.

Between these, the Zynq 7000 SoC FPGA communicates with the control Bus and the ADC communicates with the ISP to build a serial communication control system loop.

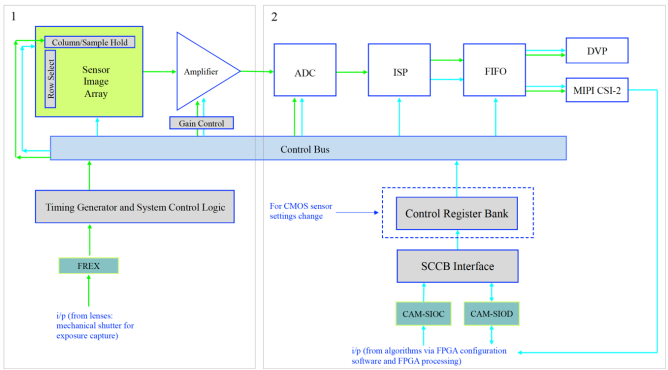


Figure 30. CMOS Sensor + Amplifier Image-Acquisition FPGA-Modulated Feedback Control System Block Diagram

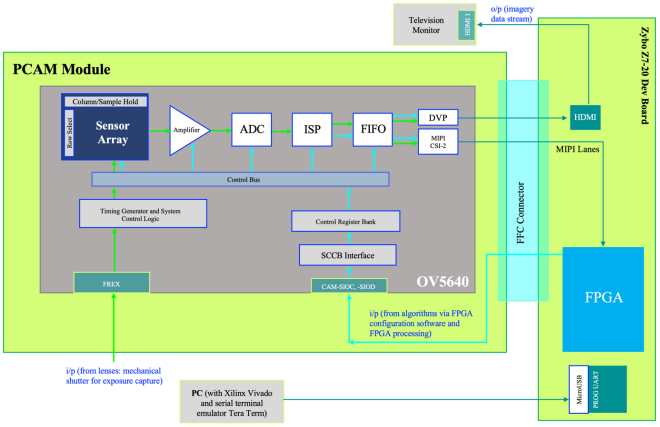


Figure 31. Macro-scaled PCAM Module to Zybo Z7-20 Development Board Control System Loop

B. ***Hardware-Software Implementation***

On the scale between control and embedded systems, the hardware-software pipeline requires parallel interfacing between the FPGA, SCCB bus, FREX bus, MIPI CSI and DVP output lanes, and memory storage and acquisition:

Figure 32. Hardware configuration of image-acquisition system using PCAM module, Zybo-Z7 development board, and display output

The Xilinx Vivado HLS software environment is used for the IP protocol to implement and synthesis the design. Each IP block represents logical processes that are connected according to the interfacing paradigm.

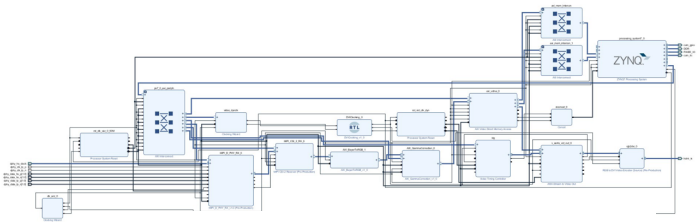


Figure 33. Zynq-7000 IP Core Block Diagram

FPGA configuration requires parallel interfacing between the configured COM port and the development board, the Xilinx Vivado protocol, implemented and synthesized design to Xilinx SDK, and a serial terminal emulator.

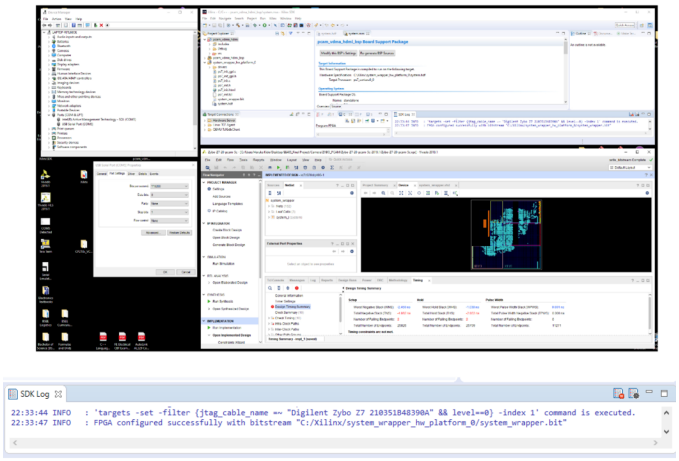


Figure 34. Xilinx Vivado and Xilinx SDK environments; Xilinx SDK log showing FPGA successfully configured

When the FPGA is successfully configured, the hardware platform is triggered and is confirmed in the SDK log.

C. *Image Properties Adjustment Example*

An example of image properties adjustment through FPGA modulation is image format change. Color spaces define the colors into realizable three-dimensional "objects" by relation between numbers and actual colors. The raw format does not have a color space as it is just the digitized pixels that make up the pixels in an image. "*Another common format is RGB; for single chip sensors with a color filter array, the pixels are interpolated to give a full color value for each pixel. As the human eye has a higher spatial resolution to brightness than to color, it is common to convert the image to YCbCr* (Brown and Shepherd, 1995)." The theory of color-space conversion is explored through the application of state-space modeling in Simulink, whereby the RGB to YCbCr conversion matrix is used in implementation of the parameterization of variables in vector-matrix form. Taking A and B parameters from the color pixel complex matrix from RGB to YCbCr, assumed variables for C and D are assigned to see a resulting time response of a presumable state-space model. The time response result is generated but is not without a "derivative error," for a "possible singularity in the solution," which may indicate BIBO instability (an unbounded response) and mean that further application of Calculus extrapolations is necessary to meet requirements of color state-space conversion theory.

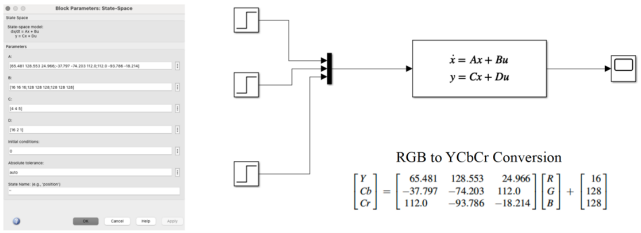


Figure 35. Example of state-space model implementation in Simulink, Parameters adjustment, and RBG to YCbCr Conversion matrix

In the serial terminal emulator Tera Term, the FPGA is triggered to change output data through the image-processing control pipeline after selecting a PCAM properties adjustment option. The selected option for this example is "d. Change Image Format <Raw or RGB>" to "1. Select image format to be RGB, output still Raw."

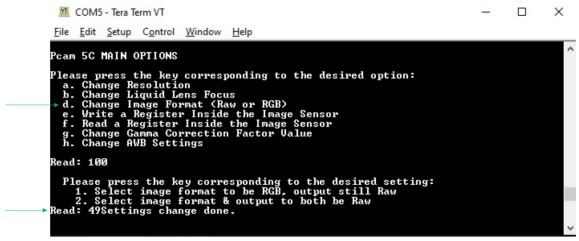


Figure 36. Zynq 7000 FPGA programming through Tera Term for image properties adjustment example: RAW to RGB conversion

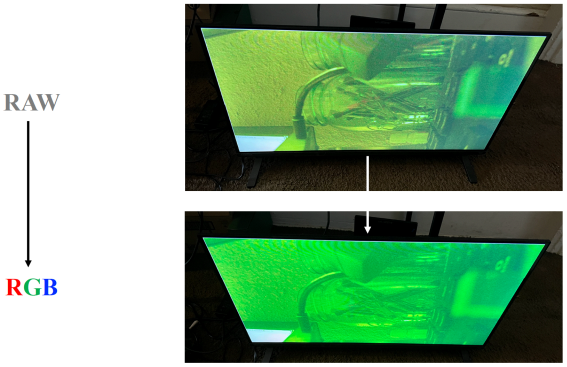


Figure 37. Display outputs before and after RAW to RGB conversion

VIII. CONCLUSION

The project serves as a foundation for both theoretical analysis and experimental application of the CMOS Sensor Image-Acquisition and Image-Processing Control System Architecture, specifically an introduction to the serial communication pipeline with FPGA modulation, using the image property of image format adjustment as an example. Applications of FPGA modulation of CMOS sensor properties extend far beyond mere photographic generation. For further applicable mathematical analysis, research on gain effects in analog-digital processing and advanced Calculus theories underlying the principles of image-acquisition may have to be explored to understand the theoretical depth of camera technology phenomena. Possible future development for the embedded systems include: [1] FPGA programming

proficiency in VHDL scripting, [2] research and implementation of DSP Algorithm, Specification Tools: HDL Coder in MATLAB/Simulink < System Generator in MATLAB/Simulink < C/C++ in Vivado HLS > RTL in Vivado (using VHDL) > DSP Hardware Platforms < HDL Coder in MATLAB/Simulink, [3] electromechanical control of lens actuator unit, [4] wireless machine image data transmission (via PMOD ethernet port), [5] LCD output screen (touchscreen), and [6] exploration of holographic voxels as three-dimensional images.

REFERENCES AND FOOTNOTES

REFERENCES

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